Patent
Attorney's Docket No. MP0042.CIP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: Tan V. MAI
Yat-Tung LAM, et al.	)	Group Art Unit: 2124
Application No.: 09/761,190	)	Appeal No. _____
Filed: January 18, 2001	)	Confirmation No.: 4662
For: MOVABLE TAP FINITE IMPULSE RESPONSE FILTER	)	Date: July 25, 2005

BRIEF FOR APPELLANT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal is from the decision of the Patent Examiner dated April 27, 2005, finally rejecting Claims 1-8, 26-33, 51-55, 61-63, 66, and 67, which are reproduced as an Appendix to this Appeal Brief.

07/27/2005 HALI11 00000087 09761190
02 FC:1402 500.00 OP

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I. Real Party in Interest

The entire interest in the present application, and the invention to which it is directed, is assigned to Marvell International Ltd., as recorded in the Patent and Trademark Office at Reel 011487, Frame 0315 and Reel 011487, Frame 0296.

II. Related Appeals and Interferences

The Appellants' legal representative and assignee do not know of any other appeals or interferences which will directly affect, or be directly affected by, or have a bearing on the Board's decision in this Appeal.

III. Status of Claims

The present application contains claims 1-8, 26-33, 51-55, and 61-69, all of which are currently pending. Claims 9-25, 34-50, and 56-60 have been canceled. Claims 64, 65, 68, and 69 have been withdrawn from consideration. Claims 1-8, 26-33, 51-55, 61-63, 66, and 67 form the basis for this Appeal.

IV. Status of Amendments

No amendments or responses were filed subsequent to final rejection.

V. Summary of the Invention

The present invention relates to a finite impulse response filter, and particularly to such a filter in which a delay in a portion thereof has an adjustable or selectable delay period, and to an echo canceller and an Ethernet transceiver including such an FIR filter. [*see* Present Application, page 1, paragraph 0006]

Finite impulse response (FIR) filters are extremely versatile digital signal processors that are used to shape and otherwise to filter an input signal so as to obtain an output signal with desired characteristics. FIR filters can be used in such diverse fields as Ethernet transceivers, read circuits for disk drives, ghost cancellation in broadcast and cable TV transmission, channel equalization for communication in magnetic recording, echo cancellation, estimation/prediction for speech processing, adaptive noise cancellation, etc. [*see* Present Application, paragraph 0008]

Typically, an FIR filter is constructed in multiple stages, with each stage including an input, a multiplier for multiplication of the input signal by a coefficient, and a summer for summing the multiplication result with the output from an adjacent stage. The coefficients are selected by the designer so as to achieve the filtering and output characteristics desired in the output signal. These coefficients (or filter tap weights) are often varied, and can be determined from a least mean square (LMS) algorithm based on gradient optimization. The input signal is a discrete time sequence which may be analog or digital, while the output is also a discrete time sequence which is the convolution of the input sequence and the filter impulse response, as determined by the coefficients. [*see* Present Application, paragraph 0010]

One problem inherent in FIR filters is that each stage requires a finite area on an integrated circuit chip. In some environments, the number of stages needed to provide desired output characteristics is large. [*see* Present Application, paragraph 0012] Moreover,

each FIR stage requires a finite amount of power and generates a corresponding amount of heat. [*see* Present Application, paragraph 0013] Thus, the conventional FIR filters exhibit undesirable characteristics in terms of integrated circuit manufacturing. Referring to the FIR filter of Figure 8, a least mean square (LMS) coefficient generator 50 provides a plurality of coefficients to each of a plurality of multipliers 82. For each multiplier, there are, in this instance, 13 conductors that connect it to the coefficient generator 50, as that is the number coefficients. Therefore, there are 2080 conductors connecting the coefficient generator 50 and the multipliers. This requires a significant amount of room and circuitry for the coefficient generator 50.

According to exemplary embodiments of the present invention, and as illustrated in Figure 9 of the present application, these and other problems can be overcome by sharing wirings for all of the coefficients supplied from LMS engine 50 to its corresponding tap of the FIR filter. Thus, by using shared wiring according to exemplary embodiments, a signification area savings in the die size can be achieved, allowing for smaller semiconductor chips and more efficient use of the space on these chips. [*see* Present Application, pages 24-25, paragraphs 0104-0105]

According to an exemplary embodiment of the present invention, as recited in, for example, independent claims 1 and 5 of the present application, an FIR filter includes a coefficient generator 50 to generate a plurality of coefficients, a plurality of control conductors, and a controller 55 coupled to a first end of plurality of control conductors. A shared wiring is provided having its first end coupled to the coefficient generator 50, and a second end coupled to a plurality of memory devices 80-n to store the coefficients in response to the controller 55. A plurality of multipliers are provided, in which each multiplier 82-n is responsive to its respective coefficient stored in its respective memory 80-n. Furthermore, a plurality of delay circuits 84 are provided, wherein each delay circuit 84 is responsive to an input. [*see* Present Application, Figures 9 and 10] According to a further

aspect of the present invention, as described in, for example, claims 62 and 63, the FIR filter can be used with an Ethernet transceiver. [*see* Present Application, paragraph 0045]

According to a second exemplary embodiment of the present invention, as recited in, for example, independent claim 51, a method of filtering a signal according to an embodiment of the present invention includes the steps of: (a) generating first and second coefficients; (b) synchronizing the generation of the first and second coefficients from step (a); (c) transferring a first control signal from step (b); and (d) transferring a second control signal from step (b). The method for filtering a signal according to a further embodiment of the present invention further includes the steps of: (e) providing a shared wiring for transferring the first and second coefficients; (f) inputting a signal; (g) storing the first coefficient transferred in step (e) in response to the first control signal transferred in step (c); (h) multiplying the first coefficient stored in step (g) by the signal input in step (f); (i) delaying the signal input in step (f); (j) storing the second coefficient transferred in step (e) in response to the second control signal transferred in step (d); and (k) multiplying the second coefficient stored in step (j) by the signal delayed in step (i).

According to a third exemplary embodiment of the present invention, as recited in, for example, independent claim 55, a method of filtering a signal according to an embodiment of the present invention includes the steps of: (a) generating N coefficients; (b) providing a shared wiring for transferring the N coefficients generated in step (a); (c)storing the N coefficients transferred in step (b); (d) filtering an input signal responsive to the N coefficients stored step (c); and (e) synchronizing step (a) and step (c).

Independent claims 26 and 66 of the present application recite the feature of "coefficient generator means for generating first and second coefficients."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a coefficient generator (engine), such as, for example, an LMS engine 1, 2, 3, 4, 5, 6, 7, and 50 illustrated in Figures 3, 8, 9, and 10, and described at pages 15 and 16, and paragraphs 0057 and 0059.

Independent claims 26 and 66 of the present application recite the feature of "controller means for synchronizing said coefficient generator."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a controller, such as, for example, controller 55 illustrated in Figures 9, 10 and 11, and described at pages 25 through, paragraphs, 0105, and 0107.

Independent claims 26 and 66 of the present application recite the features of "first control conductor means for transferring a first control signal from said controller means, and second control conductor means for transferring a second control signal from said controller means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed functions can be shown as, for example, a selector circuit, such as, for example, selector circuit comprised of multiplexer 122 and shift register 120 illustrated in Figure 10, and described at page 26, paragraph 0107.

Independent claims 26 and 66 of the present application recite the feature of "shared wiring means for transferring the first and second coefficients from said coefficient generator means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a common path, such as, for example, shared wirings illustrated in Figures 9 and 10, and described at pages 25 and 27, and described at paragraphs 0105 and 0107.

Independent claims 26 and 66 of the present application recite the feature of "input means for inputting a signal."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a multiplier and a delay, such as, for example, multiplier 82-1 and delay 84-2 illustrated in Figures 8, 9 and 10, and described at page 24, paragraph 0104.

Independent claims 26 and 66 of the present application recite the feature of "first memory means for storing the first coefficient transferred by said shared wiring means in response to said first control signal transferred by said first control conductor means" and "second memory means for storing the second coefficient transferred by said shared wiring means in response to said second control signal transferred by said second control conductor means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed functions can be shown as, for example, a memory, such as, for example, a memory 80-n illustrated in Figures 9 and 10, and described at page 25-27, paragraphs 0105 and 0107.

Independent claims 26 and 66 of the present application recite the feature of "first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means" and "second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed functions can be shown as, for example, a multiplier, such as, for example, multiplier 82-n illustrated in Figures 8, 9 and 10, and described at page 24 and 25, paragraphs 0104 and 0105.

Independent claims 26 and 66 of the present application recite the feature of "first delay means for delaying the signal input to said input means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a delay circuit, such as, for example, delay circuit 84-2 illustrated in Figures 8-10, and described at pages 24, 25, and 26, paragraphs 0104 and 0105.

Independent claims 30 and 67 of the present application recite the features of "coefficient generator means for generating N coefficients, one for each of the N taps."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a coefficient generator, such as, for example, an LMS engine 1, 2, 3, 4, 5, 6, 7, and 50 illustrated in Figures 3, 8, 9, and 10, and described at pages 15 and 16, and paragraphs 0057 and 0059.

Independent claims 30 and 67 of the present application recite the features of "shared wiring means for transferring the N coefficients from said coefficient generator means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, a common path, such as, for example, shared wirings illustrated in Figures 9 and 10, and described at pages 25 and 27, and described at paragraphs 0105 and 0107.

Independent claims 30 and 67 of the present application recite the features of "N memory means, each of said memory means responsive to said shared wiring means for storing a respective one of the N coefficients."

For purposes of illustration, the structure described in the specification as corresponding to the claimed functions can be shown as, for example, a memory, such as, for example, a memory 80-n illustrated in Figures 9 and 10, and described at page 25-27, paragraphs 0105 and 0107.

Independent claims 30 and 67 of the present application recite the features of "FIR filter means for filtering an input signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means."

For purposes of illustration, the structure described in the specification as corresponding to the claimed function can be shown as, for example, the combination of a multiplier, delay and adder. The multiplier can be shown as, for example, multiplier 82-n illustrated in Figures 8, 9 and 10, and described at page 24 and 25, paragraphs 0104 and 0105. The delay can be shown as, for example, a delay circuit, such as, for example, delay circuit 84-2 illustrated in Figures 8-10, and described at pages 24, 25, and 26, paragraphs

0104 and 0105. The adder can be shown as, for example, adder 86-2 illustrated in Figures 8-10 and described at page 25, paragraph 0104.

VI. Grounds of Rejection to be Reviewed on Appeal

The Final Office Action presents two grounds of rejection for review in this Appeal:

1. Claims 1-3, 5-8, 26-28, 30-33, 51-53, 55, 61-63, 66, and 67 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of Morrow (U.S. Patent No. 3,665,171, hereinafter "Morrow") or Sumi et al. (U.S. Patent No. 5,235,538, hereinafter "Sumi") in view of Shanks (U.S. Patent No. 3,703,632, hereinafter "Shanks").

2. Claims 4, 29 and 54 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of Morrow or Sumi in view of Shanks, further in view of Lish (U.S. Patent No. 5,050,119, hereinafter "Lish").

VII. Summary of the Arguments

For the convenience of the Board, a summary of Appellants' arguments in response to the aforementioned grounds of rejection is provided below. The following arguments are discussed in greater detail in Sections VIII.A - VIII.B.

A. Rejection of Claims 1-3, 5-8, 26-28, 30-33, 51-53, 55, 61-63, 66, and 67 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of Morrow or Sumi In View of Shanks.

1. Claims 1-3, 26-28, 51-53, 62 and 66.

These claims recites the features of an FIR filter apparatus comprising shared wiring, a first control conductor, a second control conductor, a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller, and a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller, as recited in, for example, independent claim 1 of the present application. It is respectfully suggested that neither Morrow, Sumi, nor Shanks, alone or in any combination, disclose or suggest at least those aforementioned claim features. Furthermore, it respectfully submitted that the Patent Office has failed to provide a legally sufficient motivation to combine either Morrow or Sumi with Shanks.

2. Claims 5-8, 30-33, 55, 61, 63 and 67.

These claims recite the features of an FIR filter apparatus comprising the features of a shared wiring responsive to an output of the coefficient generator, and N memories, each of

the memories responsive to the shared wiring to store a respective one of the N coefficients. It is respectfully suggested that neither Morrow, Sumi, nor Shanks, alone or in any combination, disclose or suggest at least those aforementioned claim features. Furthermore, it respectfully submitted that the Patent Office has failed to provide a legally sufficient motivation to combine either Morrow or Sumi with Shanks.

B. Rejection of Claims 4, 29, and 58 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of Morrow or Sumi in View of Shanks and Further in View of Lish.

These claims recite the feature of an FIR filter apparatus comprising the features of shared wiring, a first control conductor, a second control conductor, a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller, and a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller. It is respectfully suggested that neither Morrow or Sumi with Shanks and with Lish, alone or in any combination, disclose or suggest at least those aforementioned claim features. Furthermore, it respectfully submitted that the Patent Office has failed to provide a legally sufficient motivation to combine either Morrow or Sumi with Shanks and with Lish.

VIII. Arguments

A. Rejection of Claims 1-3, 5-8, 26-28, 30-33, 51-53, 55, 61-63, 66, and 67 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of Morrow or Sumi In View of Shanks.

1. The Morrow Patent

As understood by Appellants, Morrow is directed to a non-recursive digital filter apparatus employing delayed-add configuration. According to Morrow, by selectively altering the delay introduced by each of the delay units of a nonrecursive digital filter and by employing an alternating series of two-input adders and a partial sum delay units to perform the required addition of weight signal samples, the components of non-recursive digital filters can be considerably simplified. [*see* Morrow, Abstract]

2. The Sumi Patent

As understood by Appellants, Sumi is directed to performance of operation processing between a signal obtained by converting a coefficient into a Booth code with a Booth encoder. According to Sumi, the Booth code is stored in a memory device in advance. The stored Booth code is read out for processing an input signal in a semiconductor operation device or a digital filter. As a result, a coding operation by a Booth encoder is performed only once at the time of rewriting a coefficient and will not be repeated, thereby enabling a high-speed operation and realizing reduction of circuit scale at the same time by using an encoded Booth code directly in an operation after a coefficient has been determined. [*see* Sumi, Abstract]

3. The Shanks Patent

As understood by Appellants, Shanks is directed a recursive filter that is configured to emphasize only some of the frequency components of signals with respect to others. [*see* Shanks, Abstract] The recursive filter uses a discrete convolution device to feed back the output to the input in a particular fashion. The device uses two storage mediums, one which contains the values of the filter coefficients and the other that initially contains the input data values and (later) the computer output data values. As each output value is computed by convolving the filter coefficients with the input data values, the device stores that value back into a specific selected location in the input data storage. This causes the device on each new cycle of operation to convolve previously computed output values with the filter coefficients, along with the remaining input values. [*see* Shanks, column 3, lines 19-32]

4. Claims 1-3, 26-28, 51-53, 62 and 66.

It is respectfully submitted that the Morrow, Sumi, and Shanks, whether considered alone or in combination, do not teach or suggest an FIR filter apparatus comprising the claim features of shared wiring, *a first control conductor, a second control conductor, a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller*, and *a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller*, as recited in, for example, independent claim 1 of the present application. Furthermore, it respectfully submitted that the Patent Office has failed to provide a legally sufficient motivation to combine either Morrow or Sumi with Shanks.

a. Neither Morrow, Sumi, nor Shanks, Alone Or In Combination, Teach or Suggest All of the Features of Claims 1, 26, 51, 62 and 66.

In complete contrast to the present invention, it is respectfully submitted that neither Morrow, Sumi, nor Shanks, whether considered alone or in combination, teach or suggest the features of a shared wiring, a first control conductor, a second control conductor, a first memory *coupled to a second end of said shared wiring and coupled to a second end of said first control conductor* to store the first coefficient in response to said controller, a second memory *coupled to the second end of said shared wiring and coupled to a second end of said second control conductor* to store the second coefficient in response to said controller, as recited in, for example, independent claim 1 of the present application.

In regard to rejections made under 35 U.S.C. § 103(a), it is well known that to establish a *prima facie* case of obviousness, the prior art must disclose or suggest all of the limitations of the claims. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). As previously acknowledged by the Patent Office (in the First Office Action), neither Morrow nor Sumi disclose or suggest the feature of a shared wiring, as recited, for example, in claim 1 of the present application. In addition, it is respectfully submitted that neither Morrow nor Sumi disclose or suggest the features of: a first control conductor; a second control conductor; a first memory coupled to a second end of the shared wiring and coupled to a second end of the first control conductor to store the first coefficient in response to the controller; and a second memory coupled to the second end of the shared wiring and coupled to a second end of the second control conductor to store the second coefficient in response to the controller.

As illustrated in Figure 1 of Shanks, a second storage unit 26 is used to store the filter coefficients. According to Shanks, the second storage unit 26 "contains input contacts 27 and output contacts 28, permitting data to be selectively stored in the individual memory cells and to be selectively read out upon operation of the appropriate read control 29 and write control

30." [Shanks, column 5, lines 53-57] Write control 30 controls access to the various cells of the second storage unit 26. As disclosed by Shanks, "[i]n order to store a value into a particular preselected location (address) in the [second storage unit 26], this address in write control [30] opens appropriate gates in the [second storage unit 26] and allows the input value on line [37] to be stored in the preselected memory cell at the preselected location." [Shanks, column 4, lines 50-60, noting that "[r]ead control 29 and write control 30 physically are the same kind of units as write control 16 and read control 23," according to Shanks, column 5, lines 57-59]

Thus, it is respectfully submitted that Shanks discloses a structure fundamentally different than that recited in, for example, claim 1 of the present application. According to exemplary embodiments of the present invention, wiring is shared for *all* of the coefficients supplied from LMS engine 50 to its corresponding tap of the FIR filter. [*see* Present Application, page 25, paragraph 0105] Referring to Figure 9 of the present application, "LMS 50 supplies each of the coefficients via *a shared or common set of wirings* to a respective memory (80-1 . . . 80-n) for each corresponding tap." [Present Application, page 25, paragraph 0105 (emphasis added)] In complete contrast to the present invention, and contrary to the assertions of the Patent Office, it is respectfully submitted that line 37 illustrated in Figure 1 of Shanks is not a "shared wiring." Rather, line 37 is a *single* line that can be connected between external filter coefficient source 34 and *only one* of the memory cells of second storage unit 26 at any time using the appropriately selected contact 28. Thus, according to Shanks, to store a coefficient value in a memory cell of second storage unit 26, the contact 28 of the preselected memory cell must be engaged to allow the coefficient value to be stored in the preselected location via line 37. However, another, different contact 28 must be engaged to store a coefficient value in a different preselected memory cell via line 37.

In contrast to Shanks, the exemplary embodiments of the present invention use a shared wiring that is coupled to each of the memories. For example, claim 1 recites the

features of a first memory *coupled to a second end of the shared wiring*, and a second memory *coupled to the second end of the shared wiring*. Thus, the shared wiring is coupled to *both* the first memory and the second memory. Shanks discloses a different structure in which the line 37 can be coupled to *only one* of the memory cells of second storage unit 26 at one time, but *not more than one*.

The Patent Office, in their Final Office Action, states that

> [t]he *examiner agrees with Applicants that Shanks does not show the "wiring is shared for all of the coefficients supplied [from] the LMS engine 50 to its corresponding tap of the FIR filter*"; however Shanks is capable of providing the equivalent function because the "controller 55 '**sequentially** selects the coefficient to be provided by the LMS engine 50 and a respective memory (80-1 . . . 80-n) to store the coefficient'" It implies that the coefficient is stored in respective memory once a time [sic]. Therefore, it would have been obvious to a person having ordinary skill at the time of the invention was made to combine Shanks feature in either Morrow or Sumi et al, thereby making the claimed invention, because the proposed device is a FIR filter having 'shared wiring' for storing the desire coefficients as claimed. [Final Office Action, page 3 (emphasis in italics added, emphasis in bold and underline original)]

The Appellants respectfully submit that the Patent Office conclusions are mistaken, and evince a clear misunderstanding of the teachings of Shanks, for several reasons. For example, the Patent Office admits that Shanks does not teach or suggest the claim feature of "*a shared wiring, a first end of the shared wiring being coupled to said coefficient generator* . . . [and] a first memory *coupled to a second end of said shared wiring*." [*see*, the Present Application, claim 1] By their own admission, the Patent Office is acknowledging that it does not have and has not established a *prima facie* case of obviousness. Consequently, the Patent Office should withdraw the rejections of claims 1, 26, 51, 62 and 66 under 35 U.S.C. § 103(a). Regrettably, however, the Patent Office persists in maintaining their rejection.

Respectfully, the Appellants assert that the Patent Office either completely misunderstands the Appellants' invention, or is misconstruing the language of the claims of the present application. The language the Patent Office refers to – that the "[c]ontroller 55

sequentially selects the coefficient to be provided by LMS engine 50 and a respective memory (80-1 . . .80-n) to store the coefficient" – reflects operation on the coefficients after they have all been stored in their respective memories. As clearly illustrated in Figure 9, and described in the body of the specification, the output of the LMS engine 50 according to exemplary embodiments is connected to all memories 80-n via a shared wiring. As the Patent Office admits, Shanks does not disclose or suggest such a feature. It does not matter then how Shanks may or may not operate; it matters only that Shanks does not teach or suggest *all* the features of the claim. By the Patent Office's own admissions, Shanks discloses a system that is wholly and completely different from exemplary embodiments of the present invention.

Furthermore, the Patent Office, after acknowledging that Shanks does not teach or suggest the feature of a shared wiring, attempts to make an obvious argument that *the claim feature of shared wiring would have been obvious* from what Shanks actually does teach or suggest. Respectfully, the Appellants assert that this is an unfounded proposition of law, and note that the Patent Office has not provided any authority for such an audacious statement. In simple terms, obviousness applies only when ***all*** of the claim features are either taught or suggested, or inherent. One *cannot* use obviousness to "make up" the claim feature itself.

Consequently, it is respectfully submitted that Shanks does not disclose or suggest the features of a shared wiring, a first memory coupled to a second end of the shared wiring, and a second memory coupled to the second end of the shared wiring. Therefore, it is respectfully submitted that Shanks does not address the above-identified deficiencies of both Morrow and Sumi.

The Appellants note that in their response to the First Office action, if this rejection were to be repeated, the Patent Office was respectfully "requested to specifically point out where Morrow, Sumi or Shanks discloses or suggests these features." The Appellants respectfully note that the Patent Office has failed to provide any such citation or reference in response to the Appellants request.

b. There is No Legally Sufficient Motivation to Combine Either Morrow or Sumi In View of Shanks That Supports the Rejection of Claims 1, 26, 51, 62 and 66 Under 35 U.S.C. § 103(a).

It is respectfully submitted that the combination of the Morrow or Sumi and Shanks is wholly and completely improper. To establish a *prima facie* case of obviousness, the Examiner must show that "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead [an]individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). "The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved." *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000). The showing must be "clear and particular, and it must be supported by actual evidence." *Teleflex, Inc. v. Ficosa North American Corp.*, 299 F.3d 1313, 1334, 63 U.S.P.Q.2d 1374, 1387 (Fed. Cir. 2002) (quoting *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999)). It is not sufficient to rely on "common sense and common knowledge," as there must be specific evidence to support the motivation. *See In re Lee*, 277 F.3d. 1338, 1344-45, 61 U.S.P.Q.2d 1430, 1434-35 (Fed. Cir. 2002). In other words, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." [M.P.E.P. § 2143.01]

It is respectfully submitted the Patent Office has provided no reference, citation or other support, in Morrow, Sumi, Shanks or otherwise, for the bald and unsupported assertion that "the proposed device [of the combination of references] is a FIR filter having 'shared

wiring' for storing the desired coefficients as claimed." Again, it is respectfully submitted that the Patent Office has failed to establish a *prima facie* case of obviousness.

In the Appellants' response to the First Office Action, it was respectfully requested that should this rejection be repeated, the Patent Office was respectfully "requested to specifically provide a reference, point out a citation, or provide credible support for such a bald and unfounded assertion." The Appellants note that the Patent Office has not seen fit to provide any support whatsoever for its bald and unsupported assertion that "the proposed device [of the combination of references] is a FIR filter having 'shared wiring' for storing the desired coefficients as claimed."

In addition, according to M.P.E.P. § 2143, "[t]o establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." [M.P.E.P. § 2143.03 (emphasis added)] It is respectfully submitted that the Patent Office has utterly failed to point out where numerous features of claim 1 are allegedly taught or suggested in the combination of Morrow or Sumi and Shanks in its attempt to render the claims obvious. For example, *nowhere* in the Final Office Action does the Patent Office specify where Morrow, Sumi or Shanks teaches or suggests the features of a first control conductor and a second control conductor. In addition, *nowhere* in the Final Office Action does the Patent Office specify where Morrow, Sumi or Shanks teaches or suggests the features of a first memory coupled to a second end of the shared wiring and coupled to a second end of the first control conductor to store the first coefficient in response to the controller, and a second memory coupled to the second end of the shared wiring and coupled to a second end of the second control conductor to store the second coefficient in response to the controller.

For example, Shanks merely discloses that "[t]he external coefficient source 34 has a channel 35 which generates along with each external filter coefficient signal an address signal, which is imposed on write control 30 to locate the appropriate contact 28 for the unit cell in which a particular designated filter coefficient is to be stored." [Shanks, column 6,

lines 2-7] In other words, the Patent Office has not pointed out where or how the combination of Morrow or Sumi with Shanks discloses first and second control conductors, and first and second memories that are each coupled to the shared wiring and to an end of first and second control conductors, respectively. Consequently, it is respectfully submitted that because the Patent Office has failed to show that the combination of Morrow or Sumi with Shanks teaches or suggest each and every feature of claim 1, the Patent Office has failed to establish a *prima facie* case of obviousness.

Rather, it is respectfully submitted that the Patent Office is using impermissible hindsight in an attempt to render the claims of the present application obvious. According to M.P.E.P. § 2142, "[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art." Furthermore, according to M.P.E.P. § 2143.01, "[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of [such modification]." [citing In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990)] By stating that the motivation for combining the references in the manner suggested by the Patent Office is to "mak[e] the claimed invention," it is respectfully submitted that Patent Office has clearly and unequivocally used impermissible hindsight to re-construct Appellants' invention from the given references using Appellants' own disclosure as a template. Since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is wholly and completely founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

c. Since Neither Morrow, Sumi Nor Shanks, Alone or in Combination, Teach or Suggest All of the Features of Claims 1, 26, 51, 62 and 66, and There is No Legally Sufficient Motivation to Combine Morrow or Sumi In View of Shanks, the Combination of Morrow or Sumi with Shanks Does Not Render Independent Claims 1, 26, 51, 62 and 66 Obvious Under 35 U.S.C. § 103(a).

As the combination of Morrow or Sumi with Shanks does not teach or suggest the features of a shared wiring, a first control conductor, a second control conductor, a first memory *coupled to a second end of the shared wiring and coupled to a second end of the first control conductor* to store the first coefficient in response to the controller, and a second memory *coupled to the second end of the shared wiring and coupled to a second end of the second control conductor* to store the second coefficient in response to the controller, it is respectfully submitted that the combination of Morrow or Sumi with Shanks does not render the subject matter of claim 1 obvious.

Further, it has been shown that the motivation to combine Morrow or Sumi with Shanks is not based on anything other than impermissible hindsight reasoning.

Therefore, the rejection of independent claim 1 as unpatentable under 35 U.S.C. § 103(a) is improper and should be withdrawn.

Independent claims 26, 51, 62 and 66 recite features similar to those discussed above with respect to independent claim 1, and are, therefore, patentably distinguishable over the combination of Morrow or Sumi with Shanks for at least those reasons stated above with regard to independent claim 1.

Dependent claims 2-3, 27-28 and 52-53 variously depend from independent claims 1, 26 and 51, and are, therefore, patentably distinguishable over the combination of Morrow or Sumi with Shanks for least those reasons stated above with regard to claims 1, 26 and 51.

For at least the aforementioned reasons, it is respectfully submitted that the combination of Morrow or Sumi with Shanks does not render claims 1-3, 26-28, 51-53, 62 and 66 unpatentable.

5. Claims 5-8, 30-33, 55, 61, 63 and 67.

It is respectfully submitted that the Morrow, Sumi, and Shanks, whether considered alone or in combination, do not teach or suggest an FIR filter apparatus comprising the features of a *shared wiring* responsive to an output of the coefficient generator, and N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients, as recited in, for example, independent claim 5 of the present application. Furthermore, it respectfully submitted that the Patent Office has failed to provide a legally sufficient motivation to combine either Morrow or Sumi with Shanks.

a. Neither Morrow, Sumi, nor Shanks, Alone Or In Combination, Teach or Suggest All of the Features of Claims 5, 30 55, 61, 63 and 67.

In complete contrast to the present invention, it is respectfully submitted that neither Morrow, Sumi, nor Shanks, whether considered alone or in combination, teach or suggest the features of a *shared wiring* responsive to an output of the coefficient generator, and N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients, as recited in, for example, independent claim 5 of the present application.

As previously acknowledged by the Patent Office (in the First Office Action), neither Morrow nor Sumi disclose or suggest the feature of a shared wiring. In addition, it is respectfully submitted that neither Morrow nor Sumi disclose or suggest the features of N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients.

As discussed previously, it is respectfully submitted that Shanks discloses a structure fundamentally different than that recited in, for example, claim 5 of the present application. According to exemplary embodiments of the present invention, wiring is shared for *all* of the

coefficients supplied from LMS engine 50 to its corresponding tap of the FIR filter. [*see* Present Application, page 25, paragraph 0105] Referring to Figure 9 of the present application, "LMS 50 supplies each of the coefficients via *a shared or common set of wirings* to a respective memory (80-1 . . . 80-n) for each corresponding tap." [Present Application, page 25, paragraph 0105 (emphasis added)] In complete contrast to the present invention, and contrary to the assertions of the Patent Office, it is respectfully submitted that line 37 illustrated in Figure 1 of Shanks is not a "shared wiring." Rather, line 37 is a *single* line that can be connected between external filter coefficient source 34 and *only one* of the memory cells of second storage unit 26 at any time using the appropriately selected contact 28. Thus, according to Shanks, to store a coefficient value in a memory cell of second storage unit 26, the contact 28 of the preselected memory cell must be engaged to allow the coefficient value to be stored in the preselected location via line 37. However, another, different contact 28 must be engaged to store a coefficient value in a different preselected memory cell via line 37.

In complete contrast to Shanks, exemplary embodiments of the present invention use a shared wiring that is coupled to each of the memories. For example, claim 5 recites the feature of N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients. Thus, the shared wiring is coupled to *each* of the N memories. Shanks discloses a different structure in which the line 37 can be coupled to *only one* of the memory cells of second storage unit 26 at one time, but *not more than one.*

As discussed previously, the Patent Office has acknowledged that Shanks does not teach or suggest the claim feature of a shared wiring. By this admission, the Patent Office is acknowledging that it does not have a *prima facie* case of obviousness, and should withdraw the rejections of claims 5, 30 55, 61, 63 and 67 under 35 U.S.C. § 103(a). Regrettably, however, the Patent Office persists in maintaining their rejection.

Furthermore, the Patent Office, after acknowledging that Shanks does not teach or suggest the feature of a shared wiring, attempts to make an obvious argument that *the claim*

feature of shared wiring would have been obvious from what Shanks actually does teach or suggest. Respectfully, the Appellants assert that this is an unfounded proposition of law, and note that the Patent Office has not provided any authority for such an audacious statement. In simple terms, obviousness applies only when ***all*** of the claim features are either taught or suggested, or inherent. One *cannot* use obviousness to "make up" the claim feature itself.

Consequently, it is respectfully submitted that Shanks does not disclose or suggest the features of a *shared wiring* responsive to an output of the coefficient generator, and N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients. Therefore, it is respectfully submitted that Shanks does not address the above-identified deficiencies of both Morrow and Sumi.

b. There is No Legally Sufficient Motivation to Combine Either Morrow or Sumi In View of Shanks That Supports the Rejection of Claims 5, 30 55, 61, 63 and 67 Under 35 U.S.C. § 103(a).

It is respectfully submitted that the combination of Morrow or Sumi and Shanks is wholly and completely improper. As noted previously, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." [M.P.E.P. § 2143.01]

It is respectfully submitted the Patent Office has provided no reference, citation or other support, in Morrow, Sumi, Shanks or otherwise, for the bald and unsupported assertion that "the proposed device [of the combination of references] is a FIR filter having 'shared wiring' for storing the desired coefficients as claimed." Again, it is respectfully submitted that the Patent Office has failed to establish a *prima facie* case of obviousness.

It is again noted that in the Appellants' response to the First Office Action, if this rejection was repeated, the Patent Office was respectfully "requested to specifically provide a

reference, point out a citation, or provide credible support for such a bald and unfounded assertion." The Appellants note that the Patent Office has not seen fit to provide any support whatsoever for its bald and unsupported assertion that "the proposed device [of the combination of references] is a FIR filter having 'shared wiring' for storing the desired coefficients as claimed."

In addition, according to M.P.E.P. § 2143, "[t]o establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." [M.P.E.P. § 2143.03 (emphasis added)] It is respectfully submitted that the Patent Office has utterly failed to point out where numerous features of claim 5 are allegedly taught or suggested in the combination of Morrow or Sumi and Shanks in its attempt to render the claims obvious. For example, *nowhere* in the Final Office Action does the Patent Office specify where Morrow, Sumi or Shanks teaches or suggests the feature of N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients.

Rather, it is respectfully submitted that the Patent Office is using impermissible hindsight in an attempt to render the claims of the present application obvious. By stating that the motivation for combining the references in the manner suggested by the Patent Office is to "mak[e] the claimed invention," it is respectfully submitted that Patent Office has clearly and unequivocally used impermissible hindsight to re-construct Appellants' invention from the given references using Appellants' own disclosure as a template. Since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is wholly and completely founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

c. Since Neither Morrow, Sumi Nor Shanks, Alone or in Combination, Teach or Suggest All of the Features of Claims 5, 30 55, 61, 63 and 67, and There is No Legally Sufficient Motivation to Combine Morrow or Sumi In View of Shanks, the Combination of Morrow or Sumi with Shanks Does Not Render Independent Claims 5, 30 55, 61, 63 and 67 Obvious Under 35 U.S.C. § 103(a).

As the combination of Morrow or Sumi with Shanks does not teach or suggest the features of a *shared wiring* responsive to an output of the coefficient generator, and N memories, each of the memories *responsive to the shared wiring* to store a respective one of the N coefficients, it is respectfully submitted that the combination of Morrow or Sumi with Shanks does not render the subject matter of claim 5 obvious.

Further, it has been shown that the motivation to combine Morrow or Sumi with Shanks is not based on anything other than impermissible hindsight reasoning.

Therefore, the rejection of independent claim 5 as unpatentable under 35 U.S.C. § 103(a) is improper and should be withdrawn.

Independent claims 30, 55, 61, 63 and 67 recite features similar to those discussed above with respect to independent claim 5, and are, therefore, patentably distinguishable over the combination of Morrow or Sumi with Shanks for at least those reasons stated above with regard to independent claim 5.

Dependent claims 6-8 and 31-33 variously depend from independent claims 5 and 30, and are, therefore, patentably distinguishable over the combination of Morrow or Sumi with Shanks for least those reasons stated above with regard to claims 5 and 30.

For at least the aforementioned reasons, it is respectfully submitted that the combination of Morrow or Sumi with Shanks does not render claims 5-8, 30-33, 55, 61, 63 and 67 unpatentable.

Hence, the subject matter of these claims is separately patentable for this reason.

B. Rejection of Claims 4, 29, and 58 Under 35 U.S.C. § 103(a) as Allegedly Being Unpatentable Over the Combination of Morrow or Sumi in View of Shanks and Further in View of Lish.

It is respectfully submitted that the Morrow, Sumi, and Shanks, whether considered alone or in combination, does not teach or suggest an FIR filter apparatus comprising the features of *shared wiring*, *a first control conductor*, *a second control conductor*, a first memory *coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller*, and a second memory *coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller*. Furthermore, it respectfully submitted that the Patent Office has failed to provide a legally sufficient motivation to combine either Morrow or Sumi with Shanks and with Lish.

1. The Lish Patent.

As understood by Appellants, Lish is directed to a transversal filter that has more delay elements than adjustable multipliers. According to Lish, a switching arrangement supplies each multiplier with the signal from a selected one of a group of the elements. Each element is a member of one of the groups. The outputs of the multipliers are added, and their sum is used to control optimization of the multiplier weights for a given set of switched connections. Successive sets of connections are established to develop sets of optimized weights, until each delay element output has been used. A globally optimized set of connections and weights is then used for processing information. [*see* Lish, Abstract]

2. Neither Morrow, Sumi, Shanks, Nor Lish, Whether Considered Alone Or In Combination, Teach or Suggest All of the Features of Claims 4, 29, and 54.

In regard to rejections made under 35 U.S.C. §103(a), it is well known that to establish a prima facie case of obviousness, the prior art must disclose or suggest all of the limitations of the claims. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

For example, it is respectfully submitted that Lish does not disclose or suggest the features of a shared wiring, a first control conductor, a second control conductor, a first memory *coupled to a second end of the shared wiring and coupled to a second end of the first control conductor* to store the first coefficient in response to the controller, and a second memory *coupled to the second end of the shared wiring and coupled to a second end of the second control conductor* to store the second coefficient in response to the controller.

It is respectfully noted that *nowhere* in the Final Office Action does the Patent Office even attempt to point our or otherwise cite where Lish discloses or suggests such features.

Therefore, it is respectfully submitted that Lish does not address the above-identified deficiencies of Morrow, Sumi and Shanks.

3. There is No Legally Sufficient Motivation to Combine Either Morrow or Sumi In View of Shanks and Further In View of Lish That Supports the Rejection of Claims 4, 29 and 54 Under 35 U.S.C. § 103(a)

It is respectfully submitted that the combination of the Morrow or Sumi and Shanks and Lish is wholly and completely improper. As noted previously, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." [M.P.E.P. § 2143.01]

It is respectfully submitted the Patent Office has provided no reference, citation or other support, in Morrow, Sumi, Shanks, Lish or otherwise, for the bald and unsupported assertion that "the proposed device is a FIR filter having 'shared wiring' and 'variable delay' for storing the desired coefficients as claimed." Again, it is respectfully submitted that the Patent Office has failed to establish a *prima facie* case of obviousness.

Once again it is noted that in the Appellants' response to the First Office Action, if this rejection was repeated, the Patent Office was respectfully "requested to specifically provide a reference, point out a citation, or provide credible support for such a bald and unfounded assertion." The Appellants note that the Patent Office has yet again not seen fit to provide any support whatsoever for its bald and unsupported assertion that "the proposed device [of the combination of references] is a FIR filter having 'shared wiring' and 'variable delay' for storing the desired coefficients as claimed."

Rather, it is respectfully submitted that the Patent Office is using impermissible hindsight in an attempt to render the claims of the present application obvious. By stating that the motivation for combining the references in the manner suggested by the Patent Office is to "mak[e] the claimed invention," it is respectfully submitted that Patent Office has clearly and unequivocally used impermissible hindsight to re-construct Appellants' invention from the references using Appellants' own disclosure as a template. Since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is wholly and completely founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

4. Since Neither Morrow, Sumi, Shanks, Nor Lish, Whether Considered Alone or in Combination, Teach or Suggest All of the Features of Claims 4, 29, and 54, and There is No Legally Sufficient Motivation to Combine Morrow or Sumi In View of Shanks and Further In View of Lish, the Combination of Morrow or Sumi with Shanks and Lish Does Not Render Dependent Claims 4, 29, and 54 Obvious Under 35 U.S.C. §103(a).

As the combination of Morrow or Sumi with Shanks and Lish does not teach or suggest the features of a *shared wiring*, a first control conductor, a second control conductor, a first memory *coupled to a second end of the shared wiring and coupled to a second end of the first control conductor* to store the first coefficient in response to the controller, and a second memory *coupled to the second end of the shared wiring and coupled to a second end of the second control conductor* to store the second coefficient in response to the controller, it is respectfully submitted that the combination of Morrow or Sumi with Shanks and Lish does not render the subject matter of claims 4, 29, and 54 obvious.

Further, it has been shown that the motivation to combine Morrow or Sumi with Shanks further with Lish is not based on anything other than impermissible hindsight reasoning. Therefore, the rejection of claims 4, 29 and 54 as unpatentable under 35 U.S.C. §103(a) is improper and should be withdrawn.

In addition, it is noted that dependent claims 4, 29 and 54 variously depend from independent claims 1, 26 and 51, and are, therefore, patentably distinguishable over the combination of Morrow or Sumi with Shanks and Lish for least those reasons stated above with regard to claims 1, 26 and 51.

For at least the foregoing reasons, it is respectfully submitted that the combination of Morrow or Sumi with Shanks and Lish does not render the subject matter of claims 4, 29 and 54 obvious.

Accordingly, reconsideration and withdrawal of these grounds of rejection are respectfully requested.

Hence, the subject matter of these claims is separately patentable for this reason.

IX. Conclusion

For the reasons presented above, the rejections of the claims are not properly founded in the statute and should be reversed.

Respectfully submitted,

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APPENDIX

The Appealed Claims

1. An FIR filter apparatus comprising:

a coefficient generator to generate first and second coefficients;

a first control conductor;

a second control conductor;

a controller coupled to a first end of said first control conductor and a first end of said second control conductor;

a shared wiring, a first end of the shared wiring being coupled to said coefficient generator;

an input;

a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller;

a first multiplier responsive to the first coefficient stored in said first memory and said input;

a first delay circuit responsive to said input;

a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller; and

a second multiplier responsive to the second coefficient stored in said second memory and said first delay element.

2. An apparatus according to Claim 1,

wherein said coefficient generator generates a third coefficient,

wherein said apparatus further comprises:

a second delay circuit responsive to said first delay circuit;

a third control conductor, wherein a first end of said third control conductor is coupled to said controller;

a third memory coupled to the second end of said shared wiring and coupled to a second end of said third control conductor to store the third coefficient in response to said controller;

a third multiplier responsive to the third coefficient stored in said third memory and said second delay element.

3. An apparatus according to Claim 2, wherein said first delay circuit comprises a first time delay and said second delay circuit comprises a second time delay, wherein the first time delay is equal to the second time delay.

4. An apparatus according to Claim 2, wherein said first delay circuit comprises a first time delay and said second delay circuit comprises a second time delay, wherein the first time delay is different than the second time delay.

5. An FIR filter apparatus having N taps, N being a positive integer of at least two, said FIR filter apparatus comprising:

a coefficient generator to generate N coefficients, one for each of the N taps;

a shared wiring responsive to an output of said coefficient generator;

N memories, each of said memories responsive to said shared wiring to store a respective one of the N coefficients; and

an FIR filter comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memories.

6. An apparatus according to Claim 5, further comprising a controller to synchronize said coefficient generator with each of said N memories.

7. An apparatus according to Claim 6, further comprising a control wiring comprising N conductors, wherein a first end of each of said N conductors being coupled to said controller and a second end of each of said N conductors being coupled to a respective one of said N memories.

8. An apparatus according to Claim 7, wherein said shared wiring comprises M conductors, M being a positive integer greater than 2, and wherein said coefficient is M bits wide.

9. – 25. (Canceled)

26. An FIR filter apparatus comprising:

coefficient generator means for generating first and second coefficients;

controller means for synchronizing said coefficient generator;

first control conductor means for transferring a first control signal from said controller means;

second control conductor means for transferring a second control signal from said controller means;

shared wiring means for transferring the first and second coefficients from said coefficient generator means;

input means for inputting a signal;

first memory means for storing the first coefficient transferred by said shared wiring means in response to said first control signal transferred by said first control conductor means;

first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means;

first delay means for delaying the signal input to said input means;

second memory means for storing the second coefficient transferred by said shared wiring means in response to said second control signal transferred by said second control conductor means; and

second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means.

27. An apparatus according to Claim 26,

wherein said coefficient generator means generates a third coefficient,

wherein said apparatus further comprises:

third control conductor means for transferring a third control signal from said controller means

second delay means for delaying the signal from said first delay means

third memory means for storing the third coefficient transferred by said shared wiring means in response to said third control signal transferred by said third control conductor means; and

third multiplier means for multiplying the third coefficient stored in said third memory means by the signal delayed by said second delay means.

28. An apparatus according to Claim 27, wherein said first delay means comprises a first time delay and said second delay means comprises a second time delay, wherein the first time delay is equal to the second time delay.

29. An apparatus according to Claim 27, wherein said first delay means comprises a first time delay and said second delay means comprises a second time delay, wherein the first time delay is different than the second time delay.

30. An FIR filter apparatus having N taps, N being a positive integer of at least two, said FIR filter apparatus comprising:

coefficient generator means for generating N coefficients, one for each of the N taps;

shared wiring means for transferring the N coefficients from said coefficient generator means;

N memory means, each of said memory means responsive to said shared wiring means for storing a respective one of the N coefficients; and

FIR filter means for filtering an input signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means.

31. An apparatus according to Claim 30, further comprising controller means for synchronizing said coefficient generator means with each of said N memory means.

32. An apparatus according to Claim 31, further comprising control wiring means comprising N conductor means, wherein a first end of each of said N conductor means being coupled to said controller means and a second end of each of said N conductor means being coupled to a respective one of said N memory means.

33. An apparatus according to Claim 32, wherein said shared wiring means comprises M conductor means, M being a positive integer greater than 2, and wherein said coefficient is M bits wide.

34. – 50. (Canceled)

51. A method of filtering a signal comprising:

(a) generating first and second coefficients;

(b) synchronizing the generation of the first and second coefficients from step (a);

(c) transferring a first control signal from step (b);

(d) transferring a second control signal from step (b);

(e) providing a shared wiring for transferring the first and second coefficients;

(f) inputting a signal;

(g) storing the first coefficient transferred in step (e) in response to said first control signal transferred in step (c);

(h) multiplying the first coefficient stored in step (g) by the signal input in step (f);

(i) delaying the signal input in step (f);

(j) storing the second coefficient transferred in step (e) in response to said second control signal transferred in step (d); and

(k) multiplying the second coefficient stored in step (j) by the signal delayed in step (i).

52. A method according to Claim 51, further comprising:

(l) generating a third coefficient,

(m) transferring a third control signal from step (b);

(n) delaying the signal from step (i);

(o) storing the third coefficient transferred in step (1) in response to said third control signal transferred in step (m); and

(p) multiplying the third coefficient stored in step' (o) by the signal delayed step(n).

53. A method according to Claim 52, wherein in step (i) the signal is delayed by a first time delay, wherein in step (n) the signal is delayed by a second time delay, wherein the first time delay is equal to the second time delay.

54. A method according to Claim 52, wherein in step (i) the signal is delayed by a first time delay, wherein in step (n) the signal is delayed by a second time delay, wherein the first time delay is different than the second time delay.

55. A method of filtering a signal comprising:

(a) generating N coefficients;

(b) providing a shared wiring for transferring the N coefficients generated in step (a);

(c) storing the N coefficients transferred in step (b);

(d) filtering an input signal responsive to the N coefficients stored step (c); and synchronizing step (a) and step (c).

56. – 60. (Canceled)

61. (Original) A method of filtering a signal comprising:

(a) generating N coefficients;

(b) providing a shared wiring for transferring the N coefficients from step (a);

(c) generating a selection signal;

(d) storing the N coefficients transferred in step (b) in response to the selection generated in step (c);

(e) filtering a signal responsive to the N coefficients stored in step (d); and

(f) synchronizing step (a) with step (d).

62. An Ethernet transceiver, comprising:

an input to input an input signal into an Ethernet cable;

an output to outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR filter comprising:

a coefficient generator to generate first and second coefficients;

a first control conductor;

a second control conductor;

a controller coupled to a first end of said first control conductor and a first end of said second control conductor;

a shared wiring, a first end of the shared wiring being coupled to said coefficient generator;

an input;

a first memory coupled to a second end of said shared wiring and coupled to a second end of said first control conductor to store the first coefficient in response to said controller;

a first multiplier responsive to the first coefficient stored in said first memory and said input;

a first delay circuit responsive to said input;

a second memory coupled to the second end of said shared wiring and coupled to a second end of said second control conductor to store the second coefficient in response to said controller; and

a second multiplier responsive to the second coefficient stored in said second memory and said first delay element.

63. An Ethernet transceiver, comprising:

an input to input an input signal into an Ethernet cable;

an output to outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR apparatus having N taps, N being a positive integer of at least 2, comprising:

a coefficient generator to generate N coefficients, one for each of the N taps;

a shared wiring responsive to an output of said coefficient generator;

N memories, each of said memories responsive to said shared wiring to store a respective one of the N coefficients; and

an FIR filter comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memories.

64. (Withdrawn)

65. (Withdrawn)

66. An Ethernet transceiver, comprising:

input means for inputting an input signal into an Ethernet cable;

output means for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

FIR filter means comprising:

coefficient generator means for generating first and second coefficients;

controller means for synchronizing said coefficient generator;

first control conductor means for transferring a first control signal from said controller means;

second control conductor means for transferring a second control signal from said controller means;

shared wiring means for transferring the first and second coefficients from said coefficient generator means;

input means for inputting a signal;

first memory means for storing the first coefficient transferred by said shared wiring means in response to said first control signal transferred by said first control conductor means;

first multiplier means for multiplying the first coefficient stored in said first memory means by the signal input to said input means;

first delay means for delaying the signal input to said input means;

second memory means for storing the second coefficient transferred by said shared wiring means in response to said second control signal transferred by said second control conductor means; and

second multiplier means for multiplying the second coefficient stored in said second memory means by the signal delayed by said first delay means.

67. An Ethernet transceiver, comprising:

input means for inputting an input signal into an Ethernet cable;

output means for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

FIR apparatus means having N taps, N being a positive integer of at least 2, comprising:

coefficient generator means for generating N coefficients, one for each of the N taps;

shared wiring means for transferring the N coefficients from said coefficient generator means;

N memory means, each of said memory means responsive to said shared wiring means for storing a respective one of the N coefficients; and

FIR filter means for filtering an input signal comprising N filter stages, each one of the N filter stages being responsive to one of the N coefficients stored in a corresponding one of said N memory means.

68. (Withdrawn)

69. (Withdrawn)